

IEEE 1149.7, otherwise known as compact JTAG (cJTAG), builds upon traditional IEEE 1149.1 (JTAG) boundary scan to provide an enhanced test and debug standard that meets the demands of modern systems. cJTAG offers more functionality using fewer pins, while maintaining full compatibility with existing IEEE 1149.1-based hardware and software. cJTAG Logic, available exclusively from IPextreme, is the industry's first IEEE 1149.7-compliant synthesizable IP, providing a scalable, ready-to-integrate solution supporting all 6 classes of the IEEE 1149.7 standard.

**THE IEEE 1149.7 STANDARD**

IEEE 1149.7 defines a next-generation Test Access Port (TAP), known as TAP.7, which extends IEEE 1149.1 TAP (TAP.1) functionality in several ways. Whereas IEEE 1149.1 was originally developed as a solution for testing board-level interconnect, IEEE 1149.7 offers additional features to support increased chip integration, power management, application debug, and device programming. IEEE 1149.7 features are grouped into 6 classes, each of which is a superset of all the lower classes:

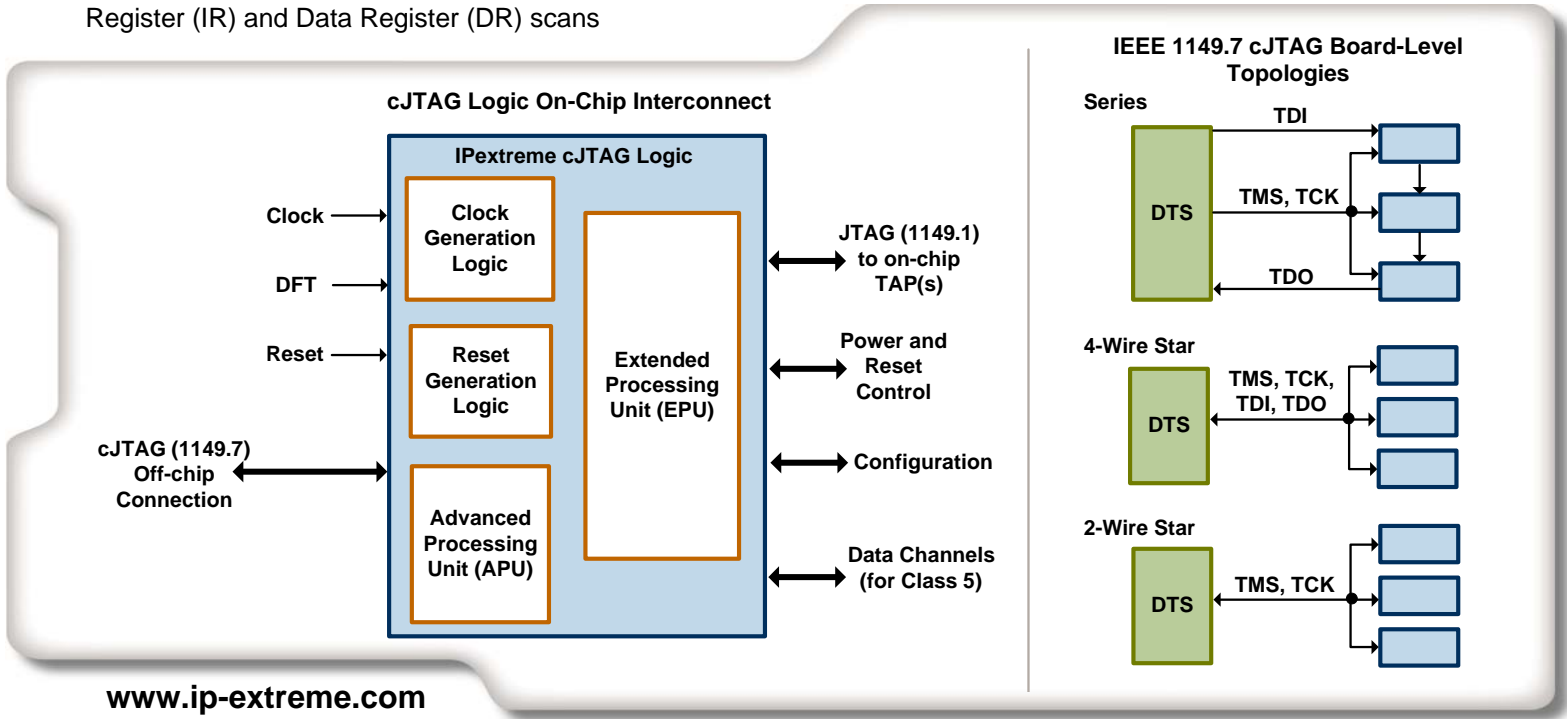
- ▶ Class 0 maintains strict compliance to 1149.1 while also providing support for multiple TAPs on a single chip
- ▶ Class 1 adds support for the 1149.7 command protocol, generation of functional and test resets, and power control
- ▶ Class 2 adds the capability to bypass a chip's system test logic, resulting in a 1-bit path for Instruction Register (IR) and Data Register (DR) scans

- ▶ Class 3 adds support for connecting TAP.7 controllers in a 4-wire star topology (TAP.7 controllers connected in parallel)
- ▶ Class 4 adds support for advanced scan protocols and 2-pin operation (all signalling done using only TMS and TCK pins), which means TDO and TDI can be removed or used for other functions
- ▶ Class 5 adds support for up to 2 data channels for non-scan data transfers, which can be used for application-specific debug and instrumentation purposes

IEEE 1149.7 does not change or replace IEEE 1149.1; instead, it offers a scalable set of extensions to IEEE 1149.1, implemented in a standard way to ensure interoperability between IEEE 1149.1 and IEEE 1149.7-based devices and test equipment.

**IPEXTREME CJTAG LOGIC FEATURES**

- ▶ Supports IEEE 1149.7 classes 0–5 (selected through hardware configuration parameter)
- ▶ Partitioned along IEEE 1149.7-specified functional boundaries (so that only the required hardware is included):
  - Extended Processing Unit (EPU) for class 0–3 operation
  - Advanced Processing Unit (APU) for class 4–5 operation
  - Further partitioning within EPU and APU for class-specific and optional features



- Separate blocks for clock and reset signal conditioning
- ▶ Supports all mandatory and optional scan formats: JScan0–3, SScan0–3, OScan0–7, and MScan
- ▶ Supports all mandatory and optional cJTAG commands
- ▶ Firewall provides robust hot-connection by disabling TCK until firewall is disabled by the Debug Test System (DTS)

## HARDWARE PARAMETERS

Several hardware parameters are available to select which cJTAG classes to support and to include or exclude hardware for optional functions:

- Class(es) supported: 0–5
- Power-down modes supported – any combination of cJTAG power-down modes:
  - Mode 0: Allow power-down if TCK remains a logic 1 for at least one millisecond.
  - Mode 1: Allow power-down in Test-Logic-Reset state if TCK remains a logic 1 for at least one millisecond
  - Mode 2: Allow power-down in Test-Logic-Reset state
  - Mode 3: No TAP.7 controller power-down
- Functional and/or test reset support
- Default cJTAG port width: 2-pin or 4-pin
- Auxiliary pin function support (available when 2-pin cJTAG port is selected)
- Support for optional scan formats: SScan0–3 and OScan2–7
- Data channel support:
  - Data channel 0/1 implemented or not
  - Data channel optional features (drain and count)

## INTERFACES

- cJTAG (1149.7) interface to off-chip DTS
- JTAG (1149.1) interface to on-chip test logic
- Power control/status interface to on-chip logic
- Functional/test reset interface to on-chip logic
- Configuration interface for node ID, JTAG device ID, decouple at startup, Controller ID, and TDI/TDO pin functions
- Data channel interface for optional data channels
- 32-kHz clock and power-on reset for cJTAG Logic, plus DFT signals to control clock and reset for scan testing

## INTEGRATING CJTAG LOGIC

The IEEE 1149.7 cJTAG interface to the off-chip DTS uses the same signals as the familiar 1149.1 TAP: TMS, TCK, TDI, TDO, and optionally TRSTn. For classes 3 and above, TDI and TDO implement additional functionality and use the names TDIC and TDOC. Likewise, for classes 4 and 5, TMS and TCK implement additional functionality and use the names TMSC and TCKC. IEEE 1149.7 also allows for a return TCK signal (RTCK) to support non-standard 1149.1 implementations where RTCK is used to modulate TCK.

The top-level interface of the IPextreme cJTAG Logic includes all required and optional cJTAG interface signals, plus the associated enable and pullup control signals for the chip-level I/O pads.

The interface to on-chip test logic is a 1149.1-compliant TAP interface for connection to a chip-level 1149.1 TAP and, optionally, multiple embedded TAPs. The 4-bit cJTAG Logic TAP state is available for the on-chip test logic to use instead of implementing an additional JTAG state machine.

Configuration inputs determine the startup functionality and can be strapped to static values, while additional optional interfaces are available for extended and advanced features such as functional/test reset, power control, and data channel support.

The size of the cJTAG Logic depends on the selected configuration. For example, a full class 4 configuration uses approximately 2500 gates.

## IPEXTREME CJTAG LOGIC DELIVERABLES

- Synthesizable Verilog source code
- Integration testbench and tests
- Documentation
- Scripts for simulation and synthesis with support for common EDA tools

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