

# IPextreme




The V1 ColdFire Processor FPGACIII, available free-of-charge from IPextreme, is the same V1 ColdFire Processor implemented in Freescale's MCF51QExx devices, but delivered to you as an SOPC Builder ready netlist optimized for the Altera Cyclone III FPGA. The V1 ColdFire Processor system bus has been adapted to the Altera AVALON bus for the FPGACIII implementation. However, there are no other changes from the standard V1 ColdFire Processor, which means the V1 ColdFire Processor FPGACIII fully supports the V1 ColdFire Instruction Set Architecture (ISA\_C) and is code-compatible with existing V1 ColdFire devices.

The V1 ColdFire Processor FPGACIII IP that you receive from IPextreme is fully compatible with Altera's SOPC Builder and Quartus II tools, which means you can quickly and easily build a system from the V1 ColdFire Processor FPGACIII and your selected peripheral IP blocks, then generate a bitfile of the whole system and program it onto your Cyclone III device. You can then download software through the V1 ColdFire single-pin debug interface and start running your application.

A free ColdFire processor on a low-cost, low-power Cyclone III FPGA gives you an ideal solution for both prototyping and production. And, should you want to migrate to an ASIC implementation in the future, you can get the same V1 ColdFire Processor from IPextreme as fully-synthesizable RTL source code.

## RESOURCES FOR HW/SW DEVELOPMENT

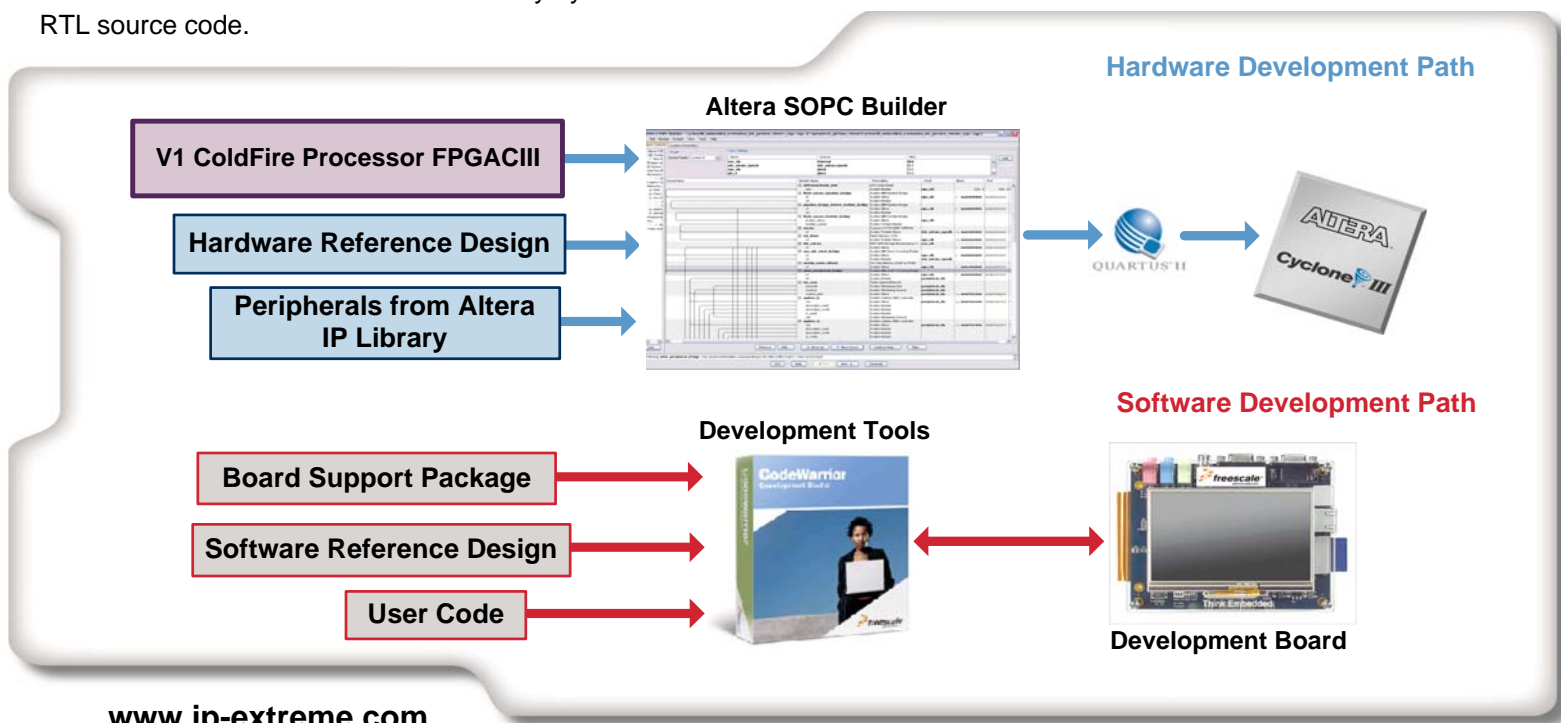
IPextreme delivers and supports the V1 ColdFire Processor FPGACIII, while resources from Altera and Freescale give you a jumpstart on hardware and software development.

### Hardware development resources from Altera:

- ▶ A rich library of peripheral IP blocks
- ▶ V1 ColdFire-based hardware reference design
- ▶ SOPC Builder for drag-and-drop IP selection and integration
- ▶ Quartus II for synthesis, place-and-route, and device programming
- ▶ Cyclone III FPGAs—low-cost 65-nm FPGAs that use 75% less power than competing FPGAs

### Software development resources from Freescale:

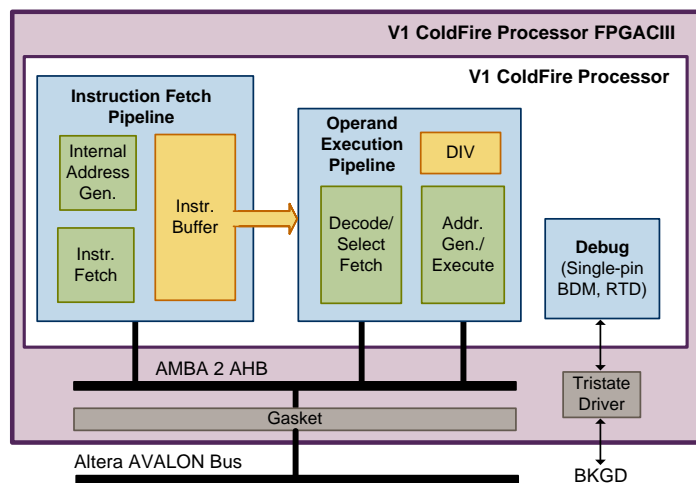
- ▶ ColdFire evaluation/development kit—a development similar to Altera's Nios II embedded evaluation kit, but containing the V1 ColdFire-based hardware reference design and equipped with a ColdFire debug connector
- ▶ CodeWarrior development tools
- ▶ Board support package
- ▶ Software reference design



## ABOUT THE V1 COLD FIRE PROCESSOR

The V1 ColdFire Processor offers a low-cost entry point to the ColdFire architecture. A simplified version of the V2 ColdFire Processor, the V1 ColdFire Processor is a low-power, low-area implementation that is fully upward compatible to higher-end ColdFire implementations such as V2, V3, and V4.

Debug support including trace and real-time debug (RTD) is through a single-wire background debug module (BDM) interface. A separate debug clock enables shut-down of debug logic when not in use.



Like all ColdFire devices, the V1 ColdFire Processor FPGACIII is supported by a rich ecosystem of development tools, software stacks, and drivers from Freescale and other leading providers such as GNU, Green Hills Software, Wind River Systems, Accelerated Technology/Mentor Graphics, and many others.

## V1 COLD FIRE PROCESSOR FEATURES

- ▶ 32-bit processor core with 24-bit address bus
- ▶ Unified instruction/data bus
- ▶ Single-wire debug interface
- ▶ Independent, decoupled pipelines
  - 2-stage Instruction Fetch Pipeline (IFP)
  - 2-stage Operand Execution Pipeline (OEP)
  - FIFO Instruction Buffer is the decoupling mechanism

- ▶ ColdFire Instruction Set Architecture Rev. C (ISA\_C)
- ▶ Variable-length RISC architecture with 16-bit, 32-bit, and 48-bit instructions
- ▶ Standard ColdFire user programming model with 16 general-purpose, 32-bit registers
- ▶ Simplified supervisor programming model supporting a supervisor stack pointer, vector base register, and CPU configuration register
- ▶ Static branch prediction mechanisms minimize change-of-flow execution time
- ▶ Execute engines include ALU, barrel shifter, and integer divider (DIV)
- ▶ Programmable response upon detection of certain illegal opcodes and illegal addresses (processor exception or system reset)

## V1 COLD FIRE DEBUG FEATURES

- ▶ ColdFire Debug B+ functionality mapped into the single-pin BDM interface
- ▶ Real time debug support, with 6 hardware breakpoints (four PC, one address, and one data) that can be configured into a 1- or 2-level trigger with a programmable response (processor halt or interrupt)
- ▶ Debug unit can use core clock (internally divided by 2) or a separate asynchronous clock

## V1 COLD FIRE PROCESSOR FPGACIII TECHNICAL SPECIFICATIONS

- ▶ Size: ~5000 LEs
- ▶ Frequency: 80 MHz (typical)

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