AUTOMOTIVE REQUIREMENTS

Integration reduces cost
Integration reduces part counts and failure points
Integration reduces power consumption and heat dissipation
Integration reduces component size
Ensured by using the same design proven in the chips from the market leader

As shown in the following table, attributes of the automotive industry drive several strict requirements on vehicle electronics that IP solutions best meet.

System-on-Chip with FlexRay IP

BMIF Bus Master Interface between Control Host Interface and memory controller
Memory DPRAM size depends on number of message buffers. FlexRay window size depends on number of message buffers, depth of Receiver FIFOs and payload data length.
FRCC2100 KEY FEATURES

- Low power consumption through extensive clock gating
- Modular design with clean CHI – PE interface for those who want to customize or develop their own Control Host Interface
- CHI clock independent of PE clock through Clock Domain Crossing, which can be removed to reduce gate count
- Compliant to FlexRay Communications Spec version 2.1A
- Single 10-Mbit/s channel for affordability, dual independent channels for 20-Mbit/s, or redundant 10-Mbit/s channels for reliability
- Data exchange (e.g., message buffer header, status, and payload) through unified or standalone shared memory
- Static message slots without buffer observable by host for debug
- Maskable interrupt signals, individual and combined
- Reports on clock synchronization
- Straightforward interface to host CPU
- One absolute timer and another absolute or relative timer
- Easily configured to best suit your application, options include:
  - Number of message buffers implemented is a hardware configuration option (4-256)
  - Message buffer setup is programmed as runtime: number of message buffers used, payload size, transmit or receive
  - Two independent receive FIFOs each with up to 255 entries and flexible filtering
  - Four configurable slot error counters

FRCC2100 IP DELIVERABLES

- Verilog RTL code of FlexRay module
- ROM image for Protocol Engine microsequencer (Motorola S-record)
- Integration testbench including:
  - 3 node FlexRay cluster communication example
  - Memory simulation models (DPRAM, SRAM, ROM)
  - Bus Driver simulation model
  - Clock and Reset Control
  - Host bus functional model
  - Bus Master Interface with interface to DPRAM
  - Configuration setup example
  - FlexRay bus sniffer
- XPack™ IP Configuration GUI to specify options and timing and automatically generate synthesis scripts and constraints
- EDA Neutral XPack packaging environment, supporting:
  - Incisive, ModelSim, and VCS-MX for verification
  - Design Compiler, RTL Compiler, BuildGates, and Precision FPGA for Synthesis

THE CUSTOMER EXPERIENCE

The IPextreme® engineering team has been creating quality IP for a decade, such as the first fully synthesizable ARM processor, the Infineon C166S, MPEG decoders, and Bluetooth. Our engineers understand integration challenges and so rework and package the design for maximum ease of use. They will typically limit parameters to those most important, simplify interfaces, bundle software, supply suites that verify connectivity, and generally transfer just the necessary knowledge from the original designers.

All the IP we ship is packaged in our patent pending XPack, which maximizes ease of use by letting the integration engineers configure complex IP through an intelligent user interface that outputs the configuration and constraints files for common tools from Cadence, Mentor, and Synopsys. During the preparation and packaging of the IP, our engineers learn enough about it to offer excellent support. IPextreme takes advantage of professional commercial IP delivery software systems and our engineers stick with the customer to ensure they successfully integrate IP purchased from us.

XPACK TECHNOLOGY

XPack is an innovative technology from IPextreme that enables customers to quickly and easily integrate IP into their designs. This lightweight IP packaging technology is based on the familiar metaphor of a datasheet, which contains all the descriptions and diagrams one would expect from a datasheet; but in reality, it is the cockpit by which users interact with the IP. Customers change parameters or modify timing information by updating fields on the interactive datasheet; XPack then automatically generates code and scripts to reflect those changes.

XPack is the result of over a decade of experience delivering IP in the manner most readily usable by customers. IPextreme packages all its products with XPack technology.

XPACK FEATURES

- Automatic configuration of source code based on user selectable options for both hardware and software parameters
- Generation of a instantiation template based on user configuration for the SoC design
- Generation of synthesis scripts and constraints for major EDA synthesis tools