



The AMBA™ Peripheral Library is a collection of AMBA 2.0 compliant subsystem building blocks providing both the AMBA bus fabric and a rich set of peripheral functions. It is the same library of AMBA platform peripherals proven in several high-volume National Semiconductor devices and is available exclusively from IPextreme.

All of the National Semiconductor AMBA AHB and APB peripherals are compliant with AMBA Specification 2.0 and are suitable for use with any AMBA 2.0 compatible controller, including the National Semiconductor CR16CP. The CR16CP is also available from IPextreme; however, AMBA the peripherals can be used with or without the CR16CP.

Several of the peripherals support DMA operation for reduced CPU utilization. For debug support, a mechanism is provided to freeze the activity of all peripherals. To help verify the connections of your assembled system, a test pattern program written in C is available to check the connections between the host processor, the AMBA bus fabric, and the connected peripherals.

Each of the peripherals has a clock-gating configuration option for low-power operation and additional configuration options for device-specific features.

### AMBA ON-CHIP BUS

The AMBA on-chip bus specification was created by ARM and version 2.0 has become a de-facto standard for system-chip developers because it is well documented and can be used without royalties. The AMBA Advanced High-Performance Bus (AHB) is for high-frequency system modules like processors and memories. The AMBA Advanced Peripheral Bus (APB) is for low-power peripheral devices.

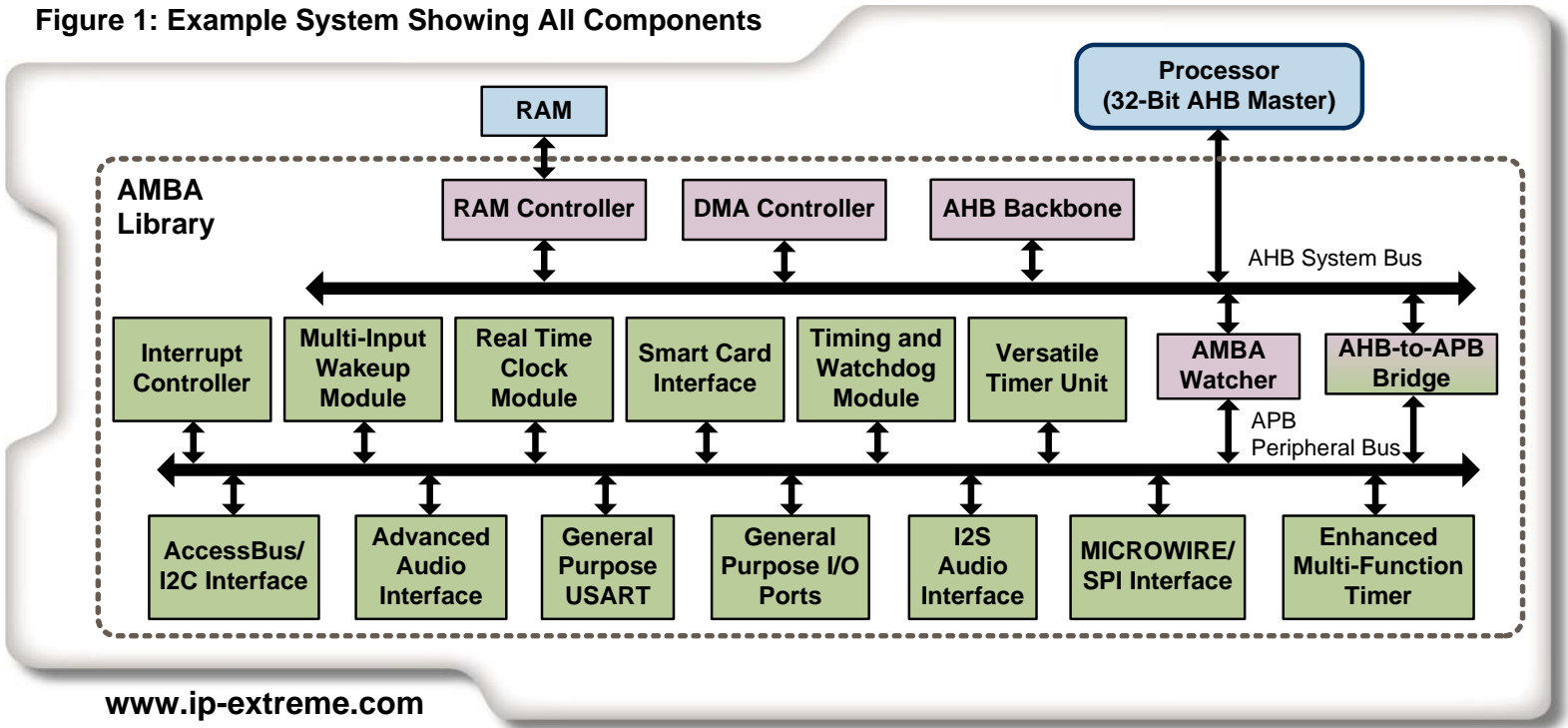
### AMBA PERIPHERAL LIBRARY: AHB PERIPHERALS

The AMBA Peripheral Library AHB peripherals provide the AMBA bus fabric as well as RAM controller and DMA controller functions.

### AHB Backbone

The AHB Backbone provides the AHB fabric to connect AHB masters and slaves. It consists of two main modules: Arbiter and Decoder.

Figure 1: Example System Showing All Components



The Arbiter ensures that only one bus master can initiate data transfers at any given time. It contains an optional register interface for allocating priorities and algorithms, and selecting the default AHB master.

The Decoder generates a select signal for the selected slave based on the address driven by the current AHB master. The Decoder supports up to 8 address regions for each slave.

### **Direct Memory Access (DMA) Controller**

The DMA Controller provides 16 independent channels (each with 4 sources) for transferring blocks of data between memory and I/O devices with minimal CPU intervention.

### **RAM Controller**

The RAM Controller enables connection of on-chip RAM to the AHB. It provides a generic interface compatible to a single-port, synchronous SRAM.

### **AHB Watcher**

The AHB Watcher monitors the AHB and logs bus errors as well as attempts to access illegal address locations by any of the AHB bus masters (for example, a CPU or DMA controller). The AHB Watcher status can be checked by polling or through a maskable interrupt.

### **AHB-to-APB Bridge**

The AHB-to-APB Bridge provides the interface between the AMBA AHB and APB, acting as a slave on the AHB and as the only bus master on the APB. It supports up to 16 APB slaves, 16- or 32-bit APB bus widths, and AHB:APB clock ratios from 1:1 to 16:1 (in integer intervals).

## **AMBA PERIPHERAL LIBRARY: APB PERIPHERALS**

The APB peripherals provide a rich set of peripheral functions enabling rapid development of complete subsystems.

### **AccessBus/I2C Interface**

The AccessBus/I2C Interface provides a two-wire serial interface compatible to the ACCESS.bus physical layer, enabling easy integration of a wide range of low-cost memories and I/O devices such

as EEPROMs, SRAMs, timers, A/D converters, D/A converters, clock chips, and peripheral drivers.

The AccessBus/I2C is also compatible with Intel's System Management Bus (SMBus) and Philips' I2C bus. It can be configured as a bus master or slave, and can maintain bidirectional communications with both multiple master and slave devices. It can be used with polling, interrupt, or DMA control.

### **Advanced Audio Interface**

The Advanced Audio Interface provides a serial, synchronous, full-duplex interface to codecs and similar serial devices. It is functionally similar to a Motorola Synchronous Serial Interface (SSI). However, it only provides a subset of a standard Motorola SSI implementation.

Features of the Advanced Audio Interface include:

- Synchronous or asynchronous receive/transmit paths
- 8- or 16-bit data words
- 16-word receive and transmit data FIFOs
- DMA support for reduced CPU utilization
- A variety of clocking and frame synchronization options

### **General Purpose USART**

The General Purpose USART module is a full-duplex synchronous/asynchronous receiver-transmitter that supports a wide range of software programmable baud rates and data formats, parity generation, error detection, flow control, and wake-up pattern detection. It can generate interrupts for several conditions—each with a separate enable—and supports DMA for both transmit and receive (also with separate enables).

### **General Purpose I/O (GPIO) Ports**

The GPIO Ports module provides two types of GPIO ports:

- Px: Bidirectional GPIO ports with two alternate functions
- Py: GPIO ports shared with a development system interface, external memory interface, or I/O expansion protocol

### I2S Audio Interface

The I2S Audio Interface provides a dedicated serial link between an APB subsystem and off-chip audio devices. The I2S Audio Interface complies with I2S Bus specification, Philips Semiconductors, February 1986 (Revised June, 1996). Features of the I2S Audio Interface include:

- Bidirectional synchronous transceiver operation in either master or slave mode
- Support for a variety of audio data widths and sample rates
- Four 8-bit FIFOs (left/right transmit and left/right receive)
- Interrupt and DMA support

### MICROWIRE/SPI Interface

The enhanced MICROWIRE/SPI interface (MWSPI) architecture is compatible with all MICROWIRE peripherals and SPI peripherals. It enables several devices to be connected on a three-wire system. At any given time, one device is the master and the others are slaves. The MWSPI module is capable of operating as either a master or a slave and in either 8-bit or 16-bit mode.

### Enhanced Multi-Function Timer

The Enhanced Multi-Function Timer is a 16-bit, multi-function timer that contains two independent 16-bit timer/counters and two 16-bit reload/capture registers. These independent timer/counters can operate from several clock sources in PWM mode, input capture mode, pulse accumulate mode, PWM pulse train mode, or just as system timers to satisfy a wide range of application requirements.

### Real Time Clock (RTC) Module

The RTC Module is a real-time counter that provides real-time information to the system. The RTC also provides alarm functions that can trigger periodic system interrupts or alternatively can be used to return the system from a low-power mode at predetermined times. Features of the RTC module include:

- Programmable input clock divider
- 16-bit prescaler counter
- 32-bit main RTC counter

- Compare registers with interrupt capability upon match
- Interrupt generation for individual events and a combined interrupt output

### Smart Card Interface

The Smart Card Interface provides a communication interface between a Smart Card and the system. The Smart Card Interface Device handles all the requirements defined in the ISO 7816-3 T=0 protocol and supports the T=1 protocol through software. Features of the Smart Card Interface include:

- 16-byte transmit/receive (half-duplex) FIFO
- Software-configurable interrupts
- DMA support for transmit and receive

### Timing and Watchdog Module

The Timing and Watchdog Module generates the clocks and interrupts used for periodic functions in the system and provides watchdog protection of software execution. Features of the Timing and Watchdog Module include:

- Programmable input clock prescaler
- 16-bit programmable interrupt timer
- 8-bit watchdog counter
- Detection and watchdog signal generation for a variety of conditions
- Watchdog freeze input
- Lock option for fully protected watchdog
- Data match mechanism for watchdog service

### Versatile Timer Unit

The Versatile Timer Unit can be configured to offer up to:

- Eight fully independent 8-bit PWM channels
- Four fully independent 16-bit PWM channels
- Eight 16-bit input capture channels

It consists of four timer subsystems, each of which contains:

- One 16-bit counter
- Two 16-bit capture/compare registers
- One 8-bit fully programmable clock prescaler

Each timer subsystem can operate in the following modes:

- Low-power mode (all clocks stopped)
- Dual 8-bit PWM mode
- 16-bit PWM mode
- Dual 16-bit input capture mode

The Versatile Timer Unit controls eight I/O pins, each of which can function either as a PWM output with programmable output polarity or as a capture input with programmable event detection and timer reset. It supports a flexible interrupt scheme with four separate system-level interrupt requests and a total of 16 interrupt sources, each with a separate interrupt pending flag and interrupt enable bit.

### Multi-Input Wakeup Module

The Multi-Input Wakeup Module provides wake-up signal interface to exit from the various low-power modes. In addition, it provides signal conditioning and grouping of external interrupt sources. A total of 32 or 64 (configuration dependent) wake-up or interrupt sources are supported.

### Interrupt Controller

The Interrupt Controller receives internal and external interrupt sources and generates maskable and non-maskable interrupts to the CPU when required. For non-maskable interrupts (NMIs), the Interrupt Controller supports:

- From 1 to 7 internal NMI sources
- External NMI
- External In-System Emulator (ISE) interrupt (optional)

The Interrupt Controller holds the status of the NMIs and generates the corresponding NMI to the CPU. For maskable interrupts, the Interrupt Controller supports:

- From 1 to 127 level-sensitive or software-triggered interrupt sources
- CPU vectored-interrupt mode
- Fixed priority allocation between interrupt sources
- Enabling/disabling of individual interrupt sources

- Polling of interrupt sources through a status register, regardless of whether the interrupts are enabled or disabled

### DELIVERABLES

The AMBA Peripherals are available for license as a Library. Each peripheral is in technology-independent RTL source code format and includes:

- Synthesizable Verilog source code
- Integration testbench
- Connectivity test patterns (in C for portability)
- Documentation
- IPextreme XPack packaging for design configuration, simulation, and synthesis with support for common EDA tools

# IPextreme

### IPextreme, Inc.

307 Orchard City Drive  
M/S 202  
Campbell, CA 95008  
800-289-6412 (toll-free)  
408-608-0421 (fax)

[www.ip-extreme.com](http://www.ip-extreme.com)

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