



CoReUse 4.5 CTAG.System (Trial Use)



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1 Introduction

1.1 Disclaimer

This trial-use standard presents the current status of a study project on a systems test access standard (CTAG.System). It should be viewed as a snapshot and not as a fully developed standard. It is intended for reviewing the concept and feasibility with the NXP DfT community. Please read and treat this document from these perspectives.

The architecture and rules for system level “Plug & Play” testability are studied in this ‘trial use’ standard, which after positive review will be introduced as a new “CTAG Plug & Play Test Access” standard.

1.2 Scope

This standard describes how “Plug-and-Play” test access could be realized for systems embedding CTAG compliant IP and CTAG “Plug & Play Test Access” compatible subsystems.

“Plug & Play Test Access” refers to the following aspects:

- The embedded CTAG IP or subsystem can be fully tested through the Test Access (Port) on the IP.
- The system integrating the CTAG IP or subsystem will have its full ATPG testability preserved
- The Test Access Infrastructure connecting all the embedded Test Access Ports is fully ATPG testable and can be (automatically) dimensioned to meet the embedded Test Access Port constraints.

Testability at the IP “leaf” level is guaranteed by the current CTAG standards for IP:

- CTAG.IP for mergeable cores
- CTAG.1500 for IEEE1500 & CTAG compliant non-mergeable cores
- CTAG.AMS as the Analog/Mixed Signal/RF extension for CTAG cores
- IEEE1500 for third-party non-mergeable cores

The concept of a Plug & Play testable Test Access Port is neither fully abstracted nor formalized in the current CTAG standards. This gives uncertainty for the integrator as minor issues like a scanchain or TestRail without bypass on a small IP can be a major issue for IC-level testability.

The CTAG.System standard is targeted to:

- Formalize the concept and use of “Plug & Play” compliant/compatible Test Access Ports (“the test access connector plugs”).
- Preserve the IP testability by the modelling of test constraints on the Test Access Port, supported by rulesets.
- Preserve the ATPG testability of the system level by modelling of the Test Access to the system/IP interface, supported by rulesets.
- Preserve the testability of systems using components compliant with the above Test Access rules by introducing a Test Access Network (TAN, “the test access

wall socket”) that matches and propagates the internal constraints to constraints on a system level Test Access Port.

- Define Test Access Ports and a Test Access Network that are ATPG testable by architecture.

The TAN will bundle multiple embedded Test Access Ports into a single Test Access Port on the system, such that the system itself is completely testable from this single port. The Test Access Ports and Test Access network together constitute a Test Access Mechanism (TAM) as defined in IEEE1500 or other core test documents.

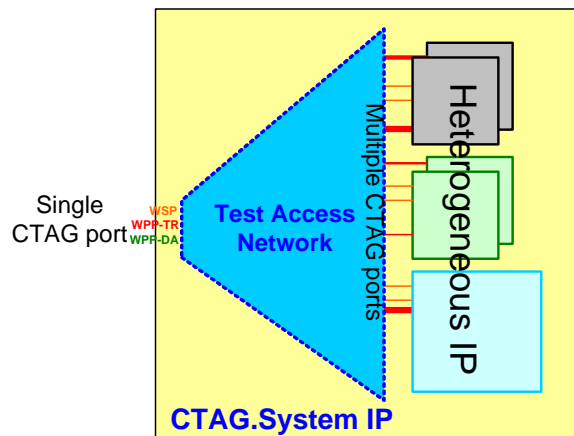
Use case:

Please note that CTAG.System has a focus on systems using CTAG compliant components and as such is not specifically targeted as an SoC standard. An SoC DfT Architect can use the concept for dimensioning the SoC TAN, but people looking for SoC DfT rules are referred to the DfT-fX initiative within NXP that focuses on best practices for SoC DfT that are used for the DfX checklist. The latest information can always be found on the DfT-fX WIKI:

<http://nww.wiki.nxp.com/display/DfTfX/DfT+for+eXcellence>.

1.3 Concepts

The CTAG.System concept of the bundling IP to a single CTAG.System compliant IP is shown in the next figure:



A collection of embedded heterogeneous IP, being CTAG.IP, CTAG.1500, CTAG.AMS all using the standard CTAG or compatible test ports is bundled together with the test access for the glue into a single CTAG test access port. From this port onward the whole collection can be treated as a single CTAG compliant IP. At the next level this procedure can be repeated. The purpose of the Test Access Network here is to bundle a collection of test access ports and requirements into a single test access port.