



CoReUse 4.5 CTAG.AMS



Table of Contents

1	Introduction	
1.1	Major changes in this release.....	9
1.2	Purpose.....	9
1.3	Scope.....	9
1.4	Intended audience.....	9
1.5	Overview.....	9
1.6	Terminology and abbreviations.....	9
2	Overview of the CTAG.AMS test strategy	
2.1	Introduction.....	11
2.2	CTAG.AMS methodology.....	11
2.3	CTAG.AMS at core-level.....	12
2.4	CTAG.AMS at chip level.....	16
3	Mixed-signal test access through the TPR	
3.1	Introduction.....	19
3.2	CTAG.AMS TPR.....	19
3.3	TPR operation modes.....	21
3.4	Core level TPR Architecture.....	23
3.5	CTAG.AMS slice types.....	24
3.6	Loading the TPR with test data.....	32
3.7	IC-level integration.....	34
4	Using CTAG.AMS in practice	
4.1	Introduction.....	37
4.2	Core level.....	37
4.3	IC-level.....	40
5	Requirements for CTAG.AMS compliant cores	
5.1	Test quality.....	43
5.2	TPR related rules.....	44
Appendix A CTAG.AMS Tool List		
A.1	Introduction.....	47
A.2	Tool List.....	47
Appendix B CTAG.AMS Open Issues		
B.1	Introduction.....	49
B.2	List of open issues.....	49

2 Overview of the CTAG.AMS test strategy

2.1 Introduction

This chapter gives an introduction into the CTAG.AMS concept, where AMS stands for Analog Mixed-Signal. CTAG.AMS is an extension of the NXP internal digital DfT standard defined by the NXP CTAG (Core Test Action Group) work group [1]. The NXP internal digital DfT standard is very close to the international standard for Embedded Core Test (IEEE 1500 [2]), and will become compliant in future.

The international standard describes core level test structures for digital testing: test access through scan-chains, test control via a wrapper instruction register (WIR) and a core wrapper to isolate the core during test operation. The nature of mixed-signal testing is different from digital: it is specification based test and not based on a fault model. This means that the traditional digital scan-based test architecture is not suited for testing mixed-signal cores. To facilitate mixed-signal testing a different test access mechanism is developed, which will be described in the next chapters. The control mechanism is the same as in the digital case, so if the mixed-signal core has scan-chains of its own their test is compliant to the digital standard.

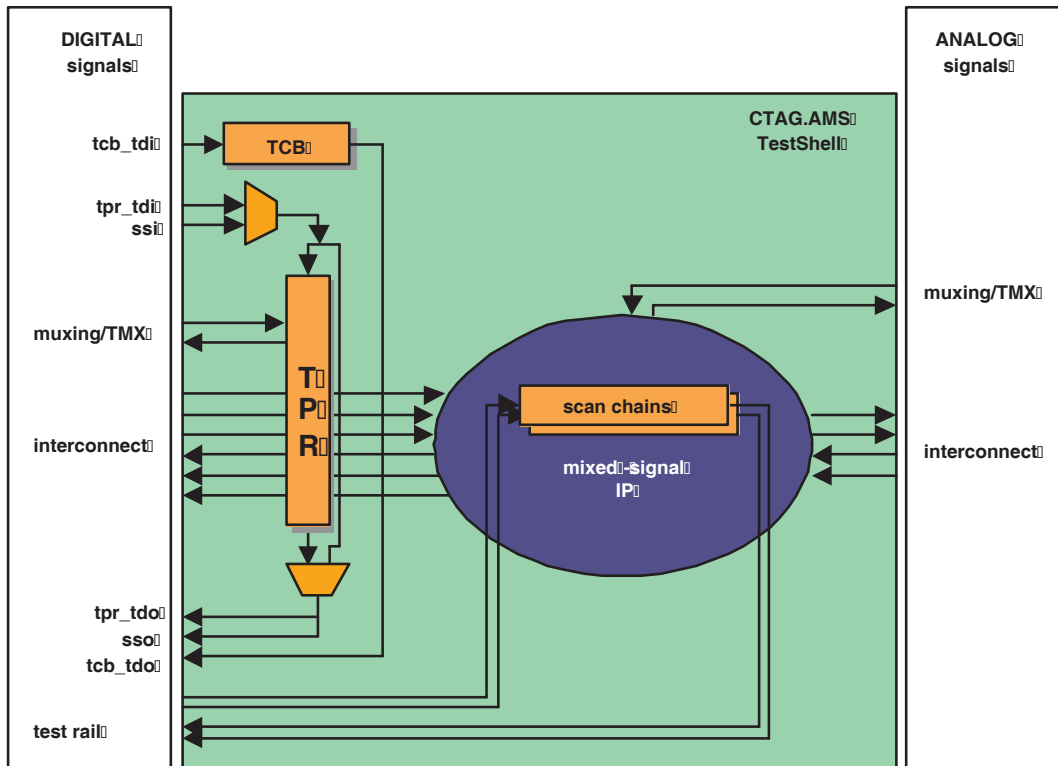
In the remainder of this document the term CTAG is used, however, one can read it as IEEE 1500.

2.2 CTAG.AMS methodology

Mixed-signal cores form an essential part of today's systems on a chip. Often these mixed-signal cores contain a number of digital signals for control and data. These digital signals can be handled in a similar way as in case of digital cores. However, there are additional requirements for mixed-signal and therefore a new access and control mechanism, CTAG.AMS, is developed to match the CTAG approach. In fact, CTAG.AMS is an extension to CTAG. Like CTAG, a mixed-signal core has a wrapper called TestShell that contains the CTAG.AMS hardware (figure 1).

It should be noted that CTAG.AMS only provides access and control for the digital signals not for the analog signals. In a lot of mixed-signal chips, the analog signals that need to be measured are already available at the IC-level pins (e.g. output of a DAC) and therefore need no specific DfT. Of course, in case that an embedded analog access is necessary, it needs to be created. That can be done, for example, using analog multiplexers. Control of such DfT, however, should be done by a CTAG compliant TCB (Test Control Block, similar to the IEEE-1500 WIR).

Figure 1. CTAG.AMS TestShell



2.3 CTAG.AMS at core-level

Test Point Register (TPR)

In case of an analog test it must be possible to isolate the core from its surrounding, provide and observe data to/from the core and support IC level interconnect test. Additionally, (at speed) functional test of the mixed-signal core may require direct (dynamic) access (e.g. streaming test data from an ADC and to a DAC). All this functionality is implemented by the so-called Test Point Register (TPR), which contains a slice (also called Test Point, TP) per mixed-signal core input/output as can be seen from figure 2.